CLAIMS

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1. Semiconductor device manufacturing method that includes a process where an insulating layer on a semiconductor substrate is etched using a mixed gas of multiple types of fluorocarbon gases that have different ratios of carbon atoms to fluorine atoms (hereafter called C/F ratio).

2. Semiconductor device manufacturing method described in Claim 1 that uses the aforementioned mixed gas where equal amounts or less of a second fluorocarbon gas with a small C/F ratio to a first fluorocarbon gas with a large C/F ratio are mixed.

3. Semiconductor device manufacturing method described in Claim 2 where C_4F_8 is used as the aforementioned first fluorocarbon gas and at least one selected from the group composed of CHF_3, CH_2F_2 and CF_4 is used as the aforementioned second fluorocarbon gas.

4. Semiconductor device manufacturing method described in Claim 1 where the aforementioned insulating layer is plasma-etched with the aforementioned mixed gas of fluorocarbon gases.

5. Semiconductor manufacturing device described in Claim 1 where a lower conducting layer is formed on the aforementioned semiconductor substrate as an electrode or wiring, a connection hole is formed by the aforementioned etching in the aforementioned insulating layer that covers this lower conducting layer, and an upper conducting layer that is connected to the aforementioned lower conducting layer is formed in the aforementioned connection hole as an electrode or wiring.

6. Semiconductor device manufacturing method described in Claim 5 where the aforementioned lower conducting layer has a titanium nitride layer on the surface where the aforementioned connection hole is formed and the aforementioned insulating layer includes a spin-on glass layer.

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7. Semiconductor device manufacturing method described in Claim 6 where the aforementioned lower conducting layer is made of a stacked structure where a titanium nitride layer, a layer of aluminum or an alloy thereof, a titanium layer, and a titanium nitride layer are stacked in that order, and the aforementioned insulating layer is made of a stacked structure where a silicon oxide layer formed from tetraethyl/orthosilicate, a spin-on glass layer, and a silicon oxide layer formed from tetraethyl/orthosilicate are stacked in that order.

8. Semiconductor device in which a lower conducting layer that has a titanium nitride layer on its surface is formed on the semiconductor substrate as an electrode or wiring, a connection hole is formed in an insulating layer that includes a spin-on glass layer to cover this lower conducting layer, and an upper conducting layer that is connected to the aforementioned lower electrode layer is formed in the aforementioned connection hole as an electrode or wiring, where the aforementioned connection hole is formed to the center position of the thickness of the aforementioned titanium nitride layer through the aforementioned insulating layer.

9. Semiconductor device described in Claim 8 where the aforementioned lower conducting layer is made of a stacked structure where a titanium nitride layer, a layer of aluminum or an alloy thereof, a titanium layer, and a titanium nitride layer are stacked in that order, and the aforementioned insulating layer is made of a stacked structure where a silicon oxide layer formed from tetraethyl orthosilicate, a spin-on glass layer, and a silicon oxide layer formed from tetraethyl orthosilicate are stacked in that order.